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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/072,165	02/07/2002	Terry C. Coughlin JR.	END920010050US1(14647)	1246

7590 02/13/2004

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EXAMINER	
CHANG, DANIEL D	

ART UNIT	PAPER NUMBER
2819	

DATE MAILED: 02/13/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/072,165	COUGHLIN ET AL.	
	Examiner	Art Unit	
	Daniel D. Chang	2819	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *20 January 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-16* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-16* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *2/7/2002* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

Acknowledgement

Receipt is acknowledged of the Amendment filed January 20, 2004.

Continued Examination Under 37 CFR 1.114

A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on January 20, 2004 has been entered.

Drawings

The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, the given set of resistance devices or the copy of given set of resistance devices must be shown or the feature(s) canceled from the claim(s). No new matter should be entered.

A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1-16 are rejected under 35 U.S.C. 102(b) as being anticipated by Lamphier et al. (US 5,666,078).

Regarding claim 9, Lamphier discloses, in Corrected Fig. 1, a circuit for controlling the impedance of an input/output cell (60) having a varying input/output impedance and including a given set of resistance devices (64, Z, 2Z, 4Z, 8Z), said circuit comprising:

a node (VZQ 31) having a variable voltage;

a copy (24, X, 2X, 4X, 8X) of said given set of resistance devices;

a comparator (30) for comparing the voltage of the node to a reference voltage (VEVAL 32);

means for adjusting (72 in Fig. 2) the voltage of the node during a defined period and according to a defined procedure, including means for activating (A0, A1, A2, A3 in Fig. 2) a number of the resistance devices of the circuit during said defined period to adjust the voltage of the node until the voltage of the node becomes within a given range of the reference voltage;

digital generator (76, 78, 82 in Fig. 2) for generating a digital signal representing the number of resistance devices activated during said defined period; and

means for transmitting (80 in Fig. 2) the digital signal to the input/output cell to adjust the input/output impedance (60).

Regarding claim 10, Lamphier discloses, in Corrected Fig. 1, that the digital generator increases a count value (4 Bit Up/Down Counter 72) during said defined period; and the

transmitting means (Impedance Update Registers 80) transmits said count value to the input/output cell after the defined period (K-Clock).

Regarding claim 11, Lamphier discloses, in Corrected Fig. 1, that the adjusting means includes:

a series of transistors (24, X, 2X, 4X, 8X) for adjusting the voltage of the node; and

means for using the count value (74 in Fig. 2) to activate said transistor in a given order to adjust the voltage of the node.

Regarding claim 12, Lamphier discloses, in Corrected Fig. 1, that the input/output cell includes a first set of transistors (64, Z, 2Z, 4Z, 8Z) for adjusting the input/output impedance;

the circuit further includes a second set of transistors (24, X, 2X, 4X, 8X) for adjusting the voltage of the node;

each of the transistors of said second set is associated (by the same 4 bits from the Counter 72) with one of the transistors in said first set;

the adjusting means (72) includes means for activating (74 and A0, A1, A2, A3) a subset of the second set of transistors to adjust the voltage of said node; and

the transmitting means (80) includes means for transmitting the digital signal (L0, L1, L2, L3) to the input/output cell to activate transistors of the first set of transistors that are associated with said subset of the second set of transistors.

Regarding claim 13, Lamphier discloses, in Corrected Fig. 1, that the input/output impedance of the input/output cell varies in a defined manner as a function of a given set of variables (col. 1, lines 21+); and

the variable voltage of said node also varies in said defined manner as a function of said given set of variables (col. 2, lines 11+).

Regarding claim 14, Lamphier discloses, in Corrected Fig. 1, that the circuit further includes a reference resistor (External RQ 22) for establishing the variable voltage at said node; and

said resistor (22) has an impedance that varies in said defined manner as a function of said given set of variables (col. 1, lines 21+; col. 2, lines 11+).

Regarding claim 15, Lamphier discloses, in Corrected Fig. 1, that adjusting means (72) includes:

means for increasing the voltage (by 4 bits A0-A3) of the node (VEVAL 32) in a first manner if the voltage of the node is less than the reference voltage; and

means for decreasing the voltage (by 4 bits A0-A3) of the node (VEVAL 32) in a second manner if the voltage of the node is more than the reference voltage (col. 2, lines 11+).

Regarding claim 16, as for the recitation, "a digital controller designed as a synthesized core or macro", it has been held that a recitation with respect to the manner in which a claimed apparatus is intended to be employed does not differentiate the claimed apparatus from a prior art apparatus satisfying the claimed structural limitations. Ex parte Masham, 2 USPQ2d 1647 (1987).

Method claims 1-8 are essentially the same in scope as apparatus claims 9-16 and are rejected similarly.

Response to Arguments

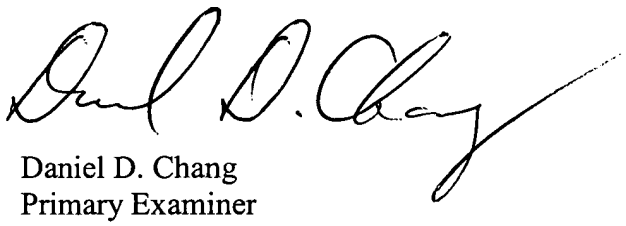
Applicant's arguments with respect to claims 1-16 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Daniel D. Chang whose telephone number is (571) 272-1801. The examiner can normally be reached on Monday through Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Michael J. Tokar can be reached on (571) 272-1812. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).



Daniel D. Chang
Primary Examiner
Art Unit 2819

DC